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Robust UHD Video Streaming Systems Using Scalable High Efficiency Video Coding

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Abstract. Among the emerging technologies in the TV industry, ultra-high definition (UHD) TV with robust video streaming is one of the most important technologies. Korea's cable TV companies opened the world's first UHD (4K resolution, 3840x2160) channel in April 2014, and Japan started the UHD service around 11 months later. Korea plans to activate UHD market with PyeongChang 2018 Winter Olympics, and Japan also has a plan to open 8K (7680x4320) UHD TV service in time for the Tokyo 2020 Olympic games.

To provide these UHD TV services over error prone networks, robust video streaming technologies including video packet error protection and error concealment (EC) are essential. However, the current video coding standard works of HEVC and SHVC (scalable HEVC) are only focusing on the video compression without careful consideration of video transmission. Besides, the MPEG-H part 1 system standard, MPEG media transport (MMT), that is considering the transmission issue also does not have any syntax and semantics for the picture priority in the same temporal level of hierarchical-B-structure and EC at all.

Regarding the EC technology, it is very difficult to find the best EC mode among multiple EC methods provided by decoder without original pictures. This is the limitation of the EC method that only works at a video decoder side. Thus, this paper proposes two main ideas; (i) a new picture prioritization method in the hierarchical B structure of HEVC, and (ii) a new EC mode signaling method that signals best EC mode(s) which is calculated and determined at an encoder side to a decoder.

In the experiments using HEVC reference model conducted, the proposed picture prioritization method shows the gains in video quality from 2.2 to 7.5 dB in Y-PSNR, and the error concealment mode signaling gains from 0.2 to 2.5 dB in Y-PSNR, with corresponding subjective improvements.

Keywords: Error Resilient Video Streaming, SHVC, HEVC, Error Concealment, Raptor FEC

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Tile Partitioning-based HEVC Parallel Processing Optimization for Asymmetric Multicore Processors

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Abstract. Recently, the necessity of parallel ultra-high definition (UHD) video processing is emerging, and the usage of the computing systems that have asymmetric processor such as ARM big.LITTLE is actively increasing. Thus, a new parallel UHD video processing method that is optimized for the asymmetric multicore systems is essential.

The next generation video coding standard HEVC introduces two parallel processing tools, Tiles and Wavefront. Among them, the Tiles divide a picture into a grid of rectangular regions that can be encoded and decoded independently. However, it does not consider computational abilities of big and LITTLE cores, and degrades the performance of multicore parallel processing.

This paper proposes a novel HEVC Tile partitioning method for the parallel processing by analyzing the computing ability of asymmetric multicores. The proposed method analyzes (i) the computing ability of asymmetric multicores and (ii) makes the regression model of computational complexity per video resolutions. Finally, the model (iii) determines the optimal HEVC Tile resolution for each core and partitions/allocates the Tiles to suitable cores.

The proposed method minimizes the gap of the decoding time between the fastest CPU core and the slowest one. Experimental results with 4K UHD official test sequences show average 20% improvement of decoding speedup on ARM asymmetric multicores system.

Keywords: HEVC, Parallel video processing, Asymmetric multicores, Tiles