Non-Uniform HEVC Tile Partitioning Method for Asymmetric Multicores

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Abstract

This paper proposes a novel high efficiency video coding (HEVC) Tile partitioning method for the parallel processing by analyzing the computing ability of asymmetric multicores. The proposed method (i) analyzes the computing ability of asymmetric multicores and (ii) makes the regression model of computational complexity per video resolutions. Finally, the model (iii) determines the optimal HEVC Tile resolution for each core and partitions/allocates the Tiles to suitable cores.

The proposed method minimizes the gap of decoding times between faster CPU cores and power-efficient cores (big/LITTLE cores). Experimental results with 4K UHD test sequences show average 20% improvement of decoding speedup on ARM asymmetric multicores system.

***Keywords*:** HEVC, Parallel processing, Asymmetric multicores, Tile

1. Introduction

Recently, multimedia contents and devices for UHD (Ultra High Definition) video are emerging actively. But, UHD video (4K and 8K) has the 4 and 16 times bigger resolution than FHD (Full High Definition) Video, and JCT-VC (Joint Collaborative Team on Video Coding) has developed a new video coding standard, named HEVC (High Efficiency Video Coding) by January 2013. The HEVC supports efficient UHD video compression and transmission in heterogeneous environments [1]. Besides, Video streaming services are also actively changing. Netflix the one of the OTT (Over-The-Top) enterprises relocated their video data from IDC (Internet Data Center) to cloud server system recently. Also, other OTT enterprises are expected too because the cloud system has better availability and scalability than IDC.

The cloud system adds new CPUs to improve their performance every year, and its internal CPUs are asymmetric with processors that have different computing abilities. For this reason, MPEG DASH (Dynamic Adaptive Streaming over HTTP) server using the cloud system needs to transcode an uploaded video to multiple bitrate bitstreams with those heterogeneous CPU clusters. In addition, ARM processors that consist of big.LITTLE asymmetric multicores are introducing these days as well [2]. However, current parallel video processing methods including HEVC Tile partition video data equally, and it degrades the decoding performance under the asymmetric computating enviroments. Thus, this paper proposes a novel HEVC Tile partitioning method for the parallel processing by analyzing the computing ability of asymmetric multicores as well as the complexity

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of video pictures. **Fig. 1** shows the conceptual diagram of proposed method.

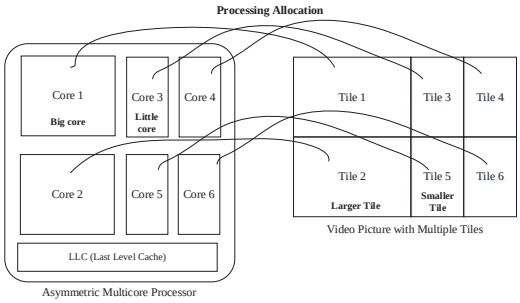

Fig. 1. Proposed Tile allocation method

2. Related Works

HEVC, the newest video coding standard, was standardized by JCT-VC in partnership with ITU-T VCEG (Video Coding Experts Group) and ISO/IEC MPEG (Moving Picture Experts Group). HEVC is based on block-based hybrid video approach as the other existing video coding standards. HEVC provides an advanced video compression capability to support a UHD video (e.g. 4K, 8K). It also provides new parallel processing tools such as Tile and WPP (Wavefront Parallel Processing).

There is the research that provides a new Tile partitioning method, which uses the number of bits of CTUs (Coding Tree Unit) [4]. The method equalizes the total number of bits in each Tiles for minimizing the decoding time differences between Tiles that have different computational complexities. Though the research is similar with our proposed method, it uses a different method to predict picture complexity and does not consider asymmetric multicore systems at all.

3. Non-Uniform Tile Partitioning Method for Asymmetric Cores

This section explains the proposed non-uniform Tile partitioning method for asymmetric cores in detail.

Fig. 2 shows the decoding time of *PeopleOn Street* sequence that consists of uniform 6 Tiles. It shows big differences between the decoding time of Tile1, Tile2 and others. In the example, Tile1 and Tile2 are allocated to big cores and other Tiles are allocated to LITTLE cores. The decoding time difference causes idle times between decoding threads.

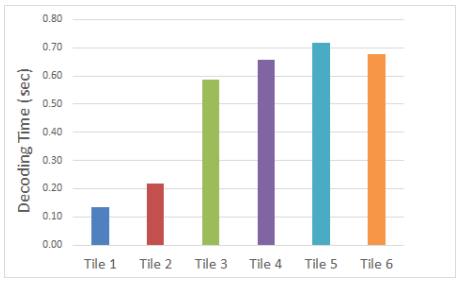

Fig. 2. Average decoding time of each Tile (test sequence: *PeopleOnStreet*)

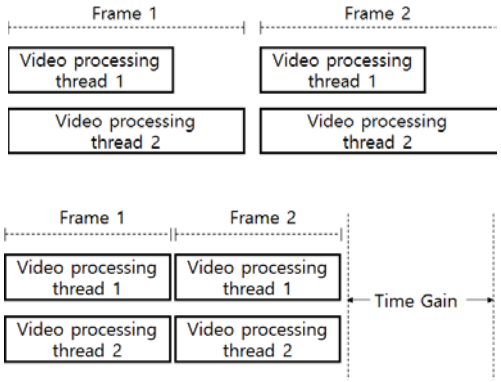

Fig. 3. Example of the decoding time gain from considering asymmetric performance ratio of big/little cores

As shown in **Fig. 3**, the problem is because the thread for the Tile that has shortest decoding time has to wait for the slowest thread(s) even if the fastest thread completes decoding job already. Thus, this paper proposes a novel Tile partitioning method considering the resolution of Tiles as well as the performance ratio of a big core and a LITTLE core. It reduces the idle time of decoding threads by partitioning and allocating non-uniform Tiles to suitable cores.

The proposed method is based on the regression model indicating a correlation between resolutions and decoding complexity [4].

As shown in Fig. 4, the proposed method (i) calculates the ratio between the decoding complexities of A' and B' based on the performance ratio of big core and little core, (ii) gets resolutions of Tiles by using complexity-resolution regression model, (iii) partitions a picture into non-uniform Tiles, (iv) allocates segmented Tiles to big and LITTLE cores.

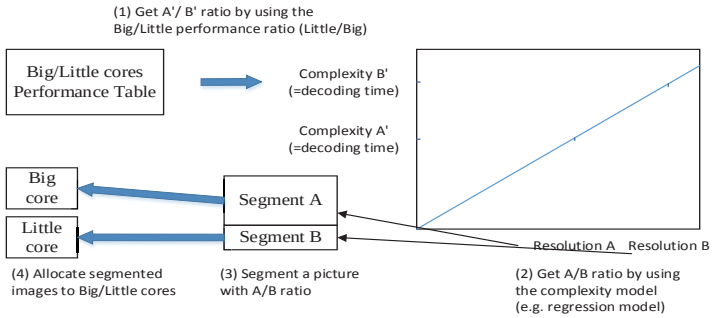

Fig. 4. The procedure of proposed method

The proposed non-uniform Tile partitioning method equalizes the decoding time of each thread, and it increases the decoding time gain.

4. Experimental Results

This paper uses HM-15.0 (HEVC Reference Model) to encode/decode test sequences on JUNO ARM development platform (asymmetric multicore platform using ARM big.LITTLE; 2 big, 4 LITTLE cores). This study modified the decoding module of HM-15.0 to allocate decoding threads to suitable cores.

Two test sequences; *PeopleOnStreet* (3840 x2160, 150 Frames) and *Traffic* (3840x2048, 300 Frames); were encoded with RA(random access), AI(all intra), and LDB(low delay B) coding structures.

Table1. Decoding time gains

Test Sequence	QP	Decoding Time Gain (%)		
		RA	AI	LDB
PeopleOn Street	22	28.11	25.81	21.80
	27	19.05	9.20	11.77
	32	17.83	14.31	7.43
	37	7.45	12.53	11.98
Traffic	22	19.55	20.74	23.35
	27	22.31	21.20	19.24
	32	25.06	16.67	19.69
	37	24.72	28.11	23.20

Table 1 shows the experimental results. The test results present that the proposed Tile partitioning method achieves decoding time gain of average 18.8% compared to uniform Tile partitioning method.

5. Conclusion

This paper proposes the a novel HEVC Tile partitioning method using asymmetric multicores for UHD parallel video processing. The proposed method minimizes the gap of decoding time between the big (faster) and LITTLE (power-efficient) cores by allocating different resolution HEVC Tiles to the cores. Experimental results with standard 4K UHD test sequences show average 20% performance improvement on ARM asymmetric multicores system. This research is also trying to increase the accuracy of HEVC Tile complexity estimation by counting prediction unit (PU) partitions in a Tile, and the performance results (around 10% more) will be explained in a next publication.

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