# Fast SW Decoding: HEVC Tile-based Parallel Decoding on Asymmetric Mobile Cores

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***Abstract*— This paper proposes a novel High Efficiency Video Coding (HEVC) Tile-based parallel processing for asymmetric multicores. The proposed method minimizes the decoding time gap between faster CPU cores and power-efficient cores. Experimental results with 4K ultra-high definition (UHD) test sequences show an average improvement of 25% in decoding speed for the most recent Android smart phones.**

***Index Terms*— HEVC, Parallel video processing, Asymmetric multicores, Tile, Decoding acceleration**

## I. INTRODUCTION

In recent years, the usage of the computing systems that have asymmetric multicore processor such as ARM big.LITTLE is actively increasing. On asymmetric multicore systems, typical uniform Tile partitioning method causes performance bottlenecks, because threads on big cores are forced to wait for threads on little cores to finish decoding of each picture. This paper proposes an optimized HEVC Tile partitioning method for asymmetric multicore systems. In addition, this paper demonstrates the proposed method on Samsung Galaxy S7 Edge smart phone.

## II. DEMONSTRATION

The proposed method works on the concept of dividing video pictures into multiple non-uniform Tiles and allocating them to big and little cores. Through the non-uniform Tile partitioning, the proposed method equalizes the relative workload between big and little cores and minimizes performance bottleneck. Fig. 1 depicts the block diagram of the proposed HEVC encoding/decoding structure.

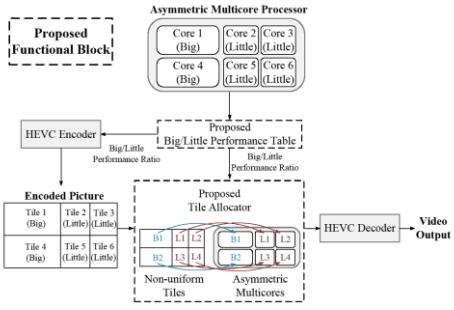


Fig. 1 Block diagram of the proposed HEVC encoding/decoding system

This paper conducts a side–by–side demonstration on two Android smart phones (Samsung Galaxy S7 Edge) which have asymmetric multicores. These two phones decode test sequences segmented by conventional uniform and the proposed non-uniform Tile partitioning methods using the proposed HEVC decoder, and this paper shows decoding speed comparison between the two phones. Figure 2 depicts side–by–side demonstration scenario to show clearly the performance improvements from the proposed method. According to our experiments with such demonstration scenario, two 4K UHD test sequences (*PeopleOnStreet* and *Traffic*) and Joint Collaborative Team on Video Coding (JCT-VC) common test conditions, the proposed method achieved an average 25% decoding time gains.

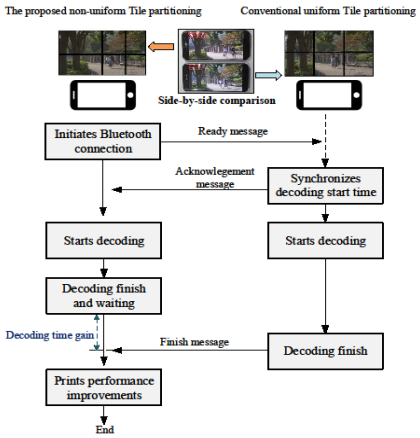


Fig. 2 Side-by-side demonstration scenario

## III. CONCLUSION

This paper optimizes Tile-based parallel video processing on asymmetric multicores. The method minimizes the decoding time gap between big (faster) and little (power efficient) cores by allocating non-uniform HEVC Tiles to the cores. Experimental results with standard 4K UHD test sequences show an average 25% performance improvement on the Android smart phone introduced recently.

## ACKNOWLEDGMENT

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Demo link: https://youtu.be/kMe3kQgmYdI